Freeform Search

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Term: L1 and ((selectively near5 connect$3) same first same second)

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Search Clear Interrupt

Search History

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L1 same ((selectively near5 connect$3) same first same second)	1	L4
L3	L1 and ((selectively near5 connect$3) same first same second)	24	L3
L2	L1 and (selectively near5 connect$3)	162	L2
L1	(serial adj1 parallel) near10 port	4210	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
"serial port" same "parallel port" and ((selectively near5 connect$3) same first same second)	57

Database:
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L6	"serial port" same "parallel port" and ((selectively near5 connect$3) same first same second)	57	L6
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L1 and ((selectively near5 connect$3) same first same second)	0	L5
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L1 same ((selectively near5 connect$3) same first same second)	1	L4
L3	L1 and ((selectively near5 connect$3) same first same second)	24	L3
L2	L1 and (selectively near5 connect$3)	162	L2
L1	(serial adj1 parallel) near10 port	4210	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and ((selectively near5 connect$3) same first same second)	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L5

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Search History

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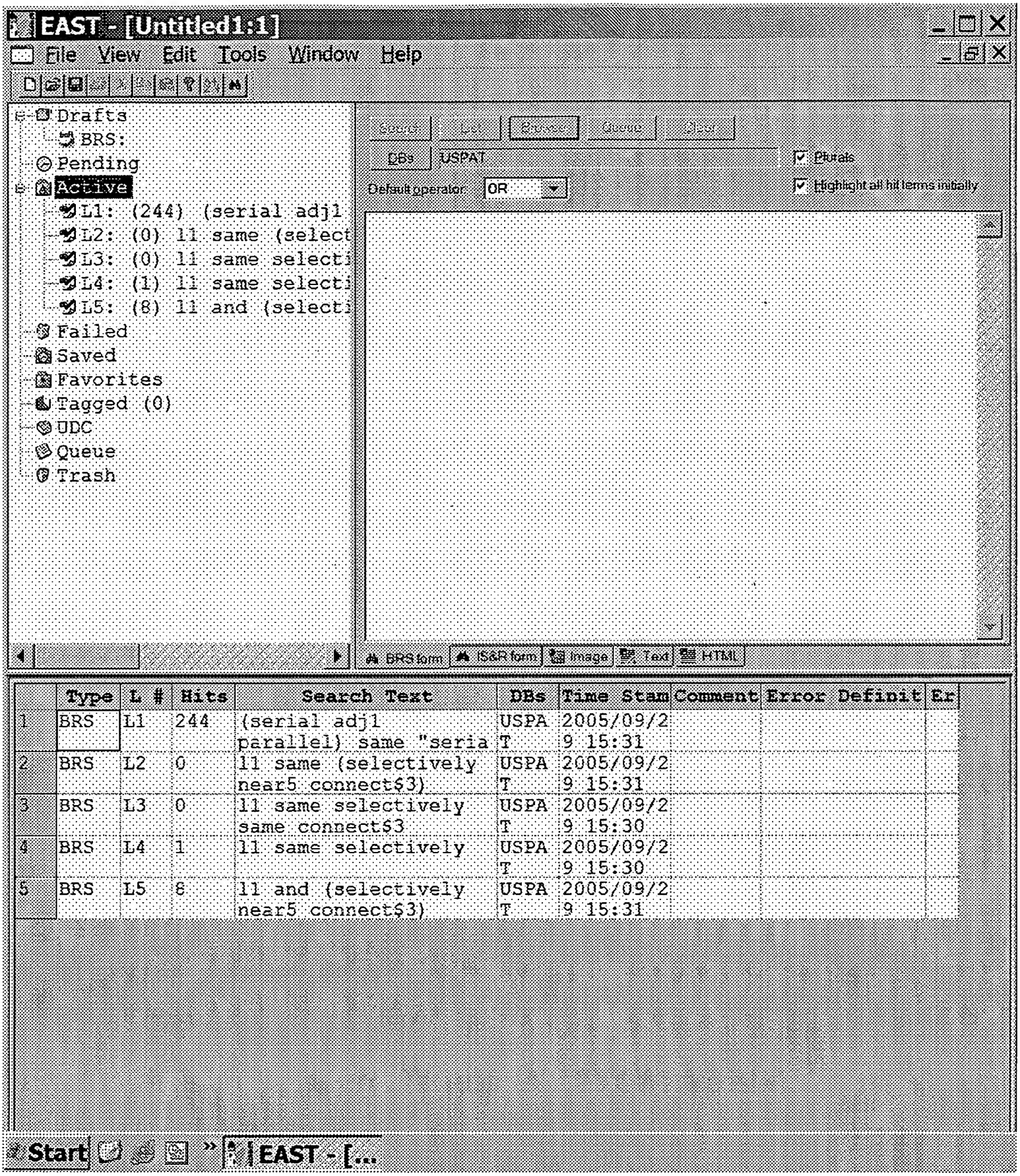
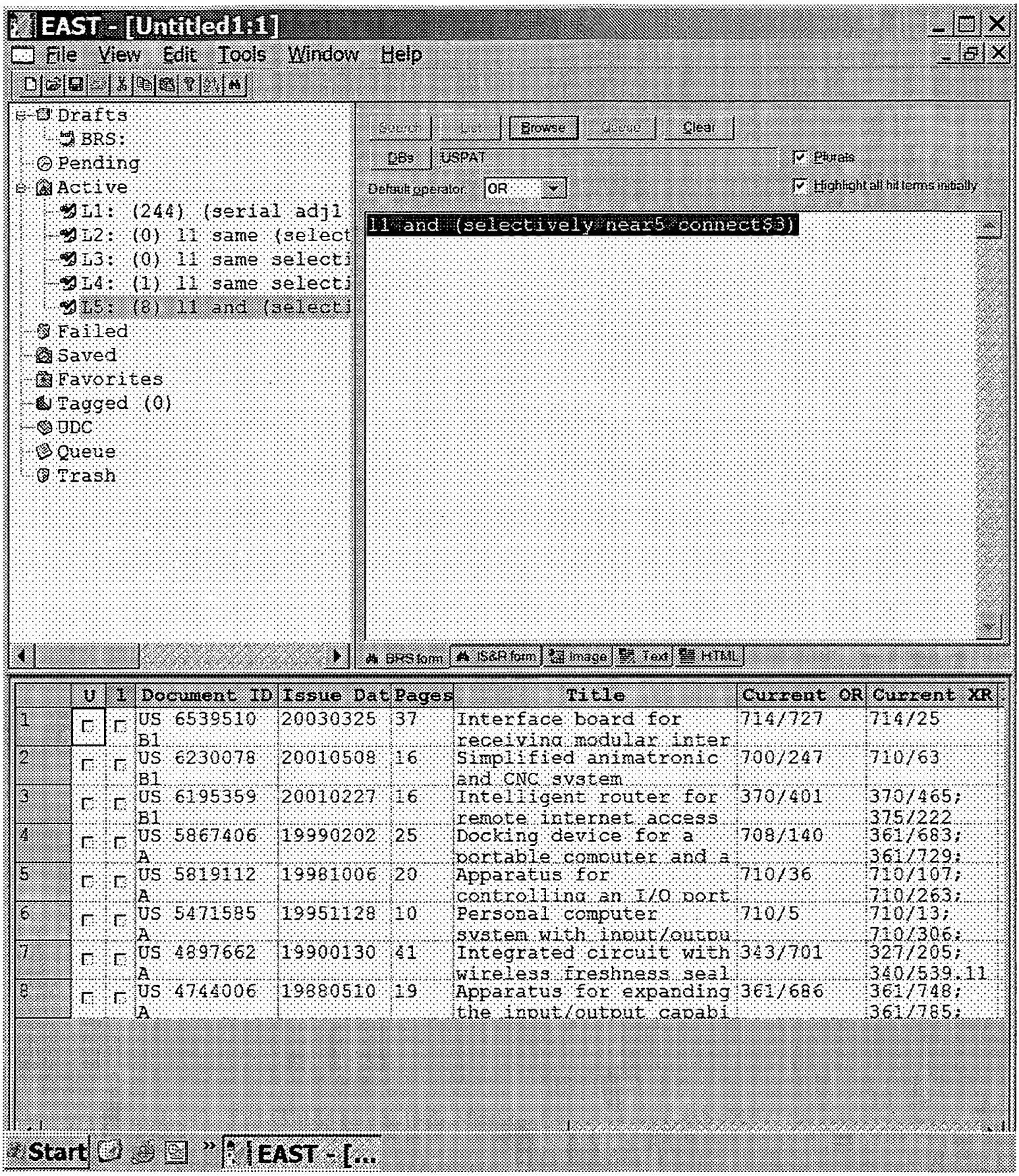
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L1 and ((selectively near5 connect$3) same first same second)	0	L5
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L1 same ((selectively near5 connect$3) same first same second)	1	L4
L3	L1 and ((selectively near5 connect$3) same first same second)	24	L3
L2	L1 and (selectively near5 connect$3)	162	L2
L1	(serial adj1 parallel) near10 port	4210	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stam	Comment	Error Definit	Er
1	BRS	L1	244	(serial adj1 parallel) same "seria	USPAT	2005/09/29 15:31			
2	BRS	L2	0	11 same (selectively near5 connect$3)	USPAT	2005/09/29 15:31			
3	BRS	L3	0	11 same selectively same connect$3	USPAT	2005/09/29 15:30			
4	BRS	L4	1	11 same selectively	USPAT	2005/09/29 15:30			
5	BRS	L5	8	11 and (selectively near5 connect$3)	USPAT	2005/09/29 15:31			


EAST - [Untitled1:1]
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Drafts
BRS:
Pending
Active
L1: (244) (serial adjl
L2: (0) l1 same (select
L3: (0) l1 same selecti
L4: (1) l1 same selecti
L5: (8) l1 and (selecti
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
l1 and (selectively near5 connect$3)
BRS form
IS&R form
Image
Text
HTML
U
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Document ID
Issue Dat
Pages
Title
Current OR
Current XR
1 US 6539510 B1 20030325 37 Interface board for receiving modular inter 714/727 714/25
2 US 6230078 B1 20010508 16 Simplified animatronic and CNC system 700/247 710/63
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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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A high speed dual port memory with simultaneous serial and random mode access for video applications

Pinkham, R. Redwine, D.J. Valente, F.A. Herndon, T.H. Anderson, D.F.

This paper appears in: **Solid-State Circuits, IEEE Journal of**
Publication Date: Dec 1984
Volume: 19 , Issue: 6
On page(s): 999 - 1007
ISSN: 0018-9200
Posted online: 2003-01-06 16:59:32.0

Abstract
A 64K/spl times/1 NMOS dynamic RAM which is interfaced in an on-chip 256-bit high-speed shift register is described. The device allows **parallel** transfer of 256 bits from a **selected** row in memory to the shift register in a normal RAS cycle time. Subsequently, the device provides simultaneous and asynchronous access from both the DRAM and the **serial** ports. The shift register can operate at a typical frequency of 33 MHz. When used in conjunction with multiple devices of the same design, a high-resolution bit-mapped video display system can be achieved with video bandwidths beyond 100 MHz. The dual-**ported** nature of the device allows a graphics processor to operate on the DRAM portion of the device while the shift register simultaneously provides a video data stream to a video display system.

Index Terms
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